ABSTRACT OF DISCLOSURE

A memory controlling apparatus which receives from an upper module of a system a command to read data from a memory module or write data in the memory module and controls accessing the memory module in response to the command. The memory controlling apparatus includes a first transmitter which transmits an address of read data or write data and the write data to a memory module via an address line; and a second transmitter which transmits data read from a memory module to the upper module of the system via a data line.